What is claimed is:

1. A semiconductor device comprising:

a substrate having a principal plane;

an insulation layer formed on said principal plane;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed therebetween;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, of which lower end is connected to one end of said heat generating layer and upper end is connected to said first wiring layer, having a cross sectional shape along said principal plane of a rectangle of which short sides are parallel to a main direction connecting said one end and the other end of said heat generating layer and long sides are parallel to a direction perpendicular to said main direction;

a second plug embedded in said insulation layer, of which lower end is connected to said other end of said heat generating layer and upper end is connected to said second wiring layer; and

a third plug embedded in said insulation layer, of which upper end is connected to said first wiring layer or said first plug and lower end reaches said principal plane.

2. The semiconductor device according to claim 1, wherein said upper end of said third plug is connected to said first plug.

3. The semiconductor device according to claim 1, wherein said substrate is a semiconductor substrate and comprises a first semiconductor layer of a first conductive type exposed to said principal plane, and a second semiconductor layer of a second conductive type selectively formed to be surrounded by said first semiconductor layer in a position directly under said third plug in said principal plane.

4. The semiconductor device according to claim 1, wherein said insulation layer is made of a low dielectric constant insulator.

5. The semiconductor device according to claim 1, wherein said first wiring layer is a wiring layer for transmitting stable potential, of which width is elongated so as to be larger than or equal to a width based on a design rule in a region including a connection portion between said first wiring layer and said first plug.

6. The semiconductor device according to claim 1, wherein length L of said long sides is set so as to satisfy a following relationship of $L \cdot S \geq 5\ \mu m \cdot D$ with respect to depth D of said first plug and length S of said short sides.

7. The semiconductor device according to claim 1, wherein said first plug is divided into a plurality of unit plugs,

a cross sectional shape of each of said plurality of unit plugs along said principal plane is a rectangle of which short sides are parallel to said main direction and long sides are parallel to a direction perpendicular to said main direction;

length S of said short sides and depth D are common with each other among said plurality of unit plugs, and

total sum L of length of said long sides of each of said plurality of unit plugs is set so as to satisfy a relationship of $L \cdot S \geq 5\ \mu m \cdot D$.

8. The semiconductor device according to claims 1, wherein length of said short sides is set in a range of 1.0 to 1.5 times of a plug width based on a design rule.

9. The semiconductor device according to claim 1, wherein a cross sectional shape of said third plug along said principal plane is a rectangle.

10. The semiconductor device according to claim 1, further comprising a fourth plug embedded in said insulation layer, of which upper end is connected to said second wiring layer or said second plug and lower end reaches said principal plane.

11. A semiconductor device comprising:

a substrate having a principal plane;

an insulation layer formed on said principal plane and made of a low dielectric constant insulator;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed therebetween;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, of which lower end is connected to one end of said heat generating layer and upper end is connected to said first wiring layer;

a second plug embedded in said insulation layer, of which lower end is connected to other end of said heat generating layer and upper end is connected to said second wiring layer; and

a third plug embedded in said insulation layer, of which upper end is connected to said first wiring layer or said first plug and lower end reaches said principal plane.

12. The semiconductor device according to claim 11, wherein said upper end of said third plug is connected to said first plug.

13. The semiconductor device according to claim 11, wherein said substrate is a semiconductor substrate and comprises a first semiconductor layer of a first conductive type exposed to said principal plane, and a second semiconductor layer of a second conductive type selectively formed to be surrounded by said first semiconductor layer in a position directly under said third plug in said principal plane.

14. The semiconductor device according to claim 11, wherein a cross sectional shape of said first plug along said principal plane is a rectangle of which short sides are parallel to a main direction connecting said one end and said other end of said heat generating layer and long sides are parallel to a direction perpendicular to said main direction.

15. The semiconductor device according to claim 11, wherein said first wiring layer is a wiring layer for transmitting stable potential, of which width is elongated so as to be larger than or equal to a width based on a design rule in a region including a connection portion between said first wiring layer and said first plug.

16. The semiconductor device according to claim 11, wherein a cross sectional shape of said third plug along said principal plane is a rectangle.

17. The semiconductor device according to claim 11, further comprising a fourth plug embedded in said insulation layer, of which upper end is connected to said second wiring layer or said second plug and lower end reaches said principal plane.

18. A semiconductor device comprising:

a semiconductor substrate having a principal plane;

an insulation layer formed on said principal plane;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed therebetween;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, of which lower end is connected to one end of said heat generating layer and upper end is connected to said first wiring layer;

a second plug embedded in said insulation layer, of which lower end is connected to other end of said heat generating layer and upper end is connected to said second wiring layer; and

a third plug embedded in said insulation layer, of which upper end is connected to said first wiring layer or said first plug and lower end reaches said principal plane, the third plug forming a Schottky barrier between the third plug and said semiconductor substrate.

19. The semiconductor device according to claim 18, wherein said upper end of said third plug is connected to said first plug.

20. The semiconductor device according to claim 18, wherein said semiconductor substrate comprises a first semiconductor layer of a first conductive type exposed to said principal plane, and a second semiconductor layer of a second conductive type selectively formed to be surrounded by said first semiconductor layer in the position directly under said third plug in said principal plane.